CLAIMS

1. A power saving circuit for use in a dynamic random access memory during refresh of the dynamic random access memory ("DRAM"), the power saving circuit comprising:

a first set of input buffers operable to generate respective internal command signals from external command signals applied to the input buffers, the input buffers in the first set being disabled by a first refresh signal;

a bias circuit operable to bias at least one internal command signal responsive to a second refresh signal; and

a refresh decoder operable to decode at least one internal command indicative of a refresh of the DRAM and causing the DRAM to be refreshed responsive thereto, the refresh decoder generating the first and second refresh signals during the refresh of the DRAM.

2. The power saving circuit of claim 1 wherein the first and second refresh signals comprise an auto-refresh signal.

3. The power saving circuit of claim 1 wherein the refresh decoder is further operable to removing the bias from the command signals and enabling the input buffers in the first set at the conclusion of the auto-refresh cycle.

4. The power saving circuit of claim 1, further comprising a clock input buffer through which an external clock signal may be applied to generate an internal clock signal, the clock input buffer being disabled by a third refresh signal, and wherein the refresh controller is operable to generate the third refresh signal during the refresh of the DRAM.

5. The power saving circuit of claim 1, further comprising a clock input buffer through which an external clock signal may be applied to generate an internal clock

signal, and wherein the refresh controller is operable to terminate the first and second refresh signals responsive to a predetermined transition of the internal clock signal.

6. The power saving circuit of claim 5 wherein the refresh controller is operable to terminate the first and second refresh signals one-half the period of the clock signal after detecting the predetermined transition.

7. The power saving circuit of claim 5 wherein the refresh controller is operable to terminate the first and second refresh signals responsive to detecting a second transition of the clock signal having a polarity that is different from the polarity of the predetermined transition.

8. The power saving circuit of claim 1 wherein the bias circuit comprises a transistor coupled to an output terminal of an input buffer in the first set through which the at least one internal command signal is coupled.

9. The power saving circuit of claim 1 wherein the bias circuit is operable to bias a plurality of internal command signals to respective states that assert a no operation memory command.

10. The power saving circuit of claim 1 wherein the refresh decoder is further operable to detect the state of a predetermined command signal, and, in response to detecting a first state of the predetermined command signal, to continue biasing the command signal and disabling the input buffers in the first set at the conclusion of the auto-refresh cycle.

11. The power saving circuit of claim 10 wherein the refresh decoder is further operable to remove the bias from the command signal and enable the input buffers in the first set responsive to detecting a transition of the predetermined command signal from the first state to a second state.

12. The power saving circuit of claim 10 wherein the refresh decoder is further operable to disable predetermined components of the dynamic random access memory at the conclusion of the auto-refresh cycle responsive to detecting a first state of the predetermined command signal.

13. The power saving circuit of claim 12 wherein the refresh decoder is further operable to enable the predetermined components of the dynamic random access memory in response to detecting a transition of the predetermined command signal from the first state to a second state.

14. The power saving circuit of claim 1 wherein the refresh decoder comprises:

a first decoder operable to decode the at least one internal command indicative of a refresh of the DRAM and to generate a predetermined refresh signal responsive thereto;

a timer coupled to the first decoder, the timer being triggered by the predetermined refresh signal and generating a refresh terminate signal a predetermined period after the predetermined refresh signal; and

a second decoder coupled to the first decoder and to the timer, the second decoder being operable to generate a refresh command and the first and second refresh signals responsive to the predetermined refresh signal, the second decoder further being operable to terminate the refresh command and the first and second refresh signals responsive to the refresh terminate signal.

15. The power saving circuit of claim 14 wherein the predetermined refresh signal comprises an auto-refresh signal and the refresh command comprises an auto-refresh command.

16. A power saving circuit for use in a dynamic random access memory during refresh of the dynamic random access memory ("DRAM"), the power saving circuit comprising:

a first set of input buffers operable to generate respective internal command signals from external command signals applied to the input buffers, the input buffers in the first set being disabled by a first refresh signal;

a clock input buffer through which an external clock signal is coupled to generate an internal clock signal;

a bias circuit operable to bias at least one internal command signal responsive to a second refresh signal; and

a refresh decoder operable to decode at least an auto-refresh command and to initiate an auto-refresh cycle responsive thereto, the refresh decoder being further operable to detect the respective states of first and second predetermined command signals, the refresh decoder being operable to:

perform a self-refresh of the DRAM in response to decoding an auto-refresh command and detecting a first state of the first predetermined command signal and a first state of the second predetermined command signal;

perform an auto-refresh of the DRAM in response to decoding an auto-refresh command and a detecting second state of the first predetermined command signal and a first state of the second predetermined command signal;

perform an auto-refresh of the DRAM and generate the first and second refresh signals in response to decoding an auto-refresh command and detecting a first state of the first predetermined command signal and a second state of the second predetermined command signal; and

perform an auto-refresh of the DRAM, generate the first and second refresh signals, and disable components of the DRAM other than the first set of input buffers at the conclusion of an auto-refresh cycle in response to decoding an auto-refresh command and detecting a second state of the first predetermined command signal and a second state of the second predetermined command signal.

17. The power saving circuit of claim 16 wherein the clock input buffer is disabled by a third refresh signal, and wherein the refresh decoder is further operable to generate the third refresh signal along with the first and second refresh signals.

18. The power saving circuit of claim 16 wherein the first predetermined signal comprises a clock enable signal.

19. The power saving circuit of claim 16 wherein the second predetermined signal comprises a data mask signal.

20. The power saving circuit of claim 16 wherein the refresh decoder is operable to terminate the first and second refresh signals at the conclusion of the auto-refresh if the first state of the first predetermined command signal and the second state of the second predetermined command signal were detected, the refresh decoder being further operable to continue generating the first and second refresh signals at the conclusion of the auto-refresh if the second state of the first predetermined command signal and the second state of the second predetermined command signal were detected.

21. The power saving circuit of claim 20 wherein the refresh decoder is operable to continue generating the first and second refresh signals at the conclusion of the auto-refresh as long as the second predetermined command signal is maintained in the second state.

22. The power saving circuit of claim 20 wherein the refresh decoder is operable to terminate the first and second refresh signals at the conclusion of the auto-refresh by detecting a predetermined transition of the internal clock signal, and to terminate the first and second refresh signals responsive to detecting the predetermined transition of the clock signal.

23. The power saving circuit of claim 22 wherein the refresh decoder is operable to wait a predetermined duration after detecting the predetermined transition terminate the first and second refresh signals before terminating the first and second refresh signals.

24. The power saving circuit of claim 16 wherein the bias circuit is operable to bias a plurality of internal command signals to generate a no operation memory command.

25. The power saving circuit of claim 16 wherein the refresh decoder comprises:

a first decoder operable to decode the at least one internal command indicative of a refresh of the DRAM and to generate a predetermined refresh signal responsive thereto;

a timer coupled to the first decoder, the timer being triggered by the predetermined refresh signal and generating a refresh terminate signal a predetermined period after the predetermined refresh signal; and

a second decoder coupled to the first decoder and to the timer, the second decoder being operable to generate a refresh command and the first and second refresh signals responsive to the predetermined refresh signal, the second decoder further being operable to terminate the refresh command and the first and second refresh signals responsive to the refresh terminate signal.

26. The power saving circuit of claim 25 wherein the predetermined refresh signal comprises an auto-refresh signal and the refresh command comprises an auto-refresh command.

27. The power saving circuit of claim 16 wherein the bias circuit comprises a transistor coupled to an output terminal of an input buffer in the first set through which the at least one internal command signal is coupled.

28. A dynamic random access memory ("DRAM"), comprising:

a row address circuit operable to receive and decoder row address signals applied to an external terminal;

a column address circuit operable to receive and decoder column address signals applied to an external terminal;

an array of dynamic random access memory cells operable to store data written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals;

a data path circuit operable to couple data signals corresponding to the data between the array and an external data terminal;

a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to respective external terminals and coupled thorough a first set of input buffers to generate respective internal command signals, the input buffers in the first set being disabled by a first refresh signal, the command signal generator further including a bias circuit operable to bias at least one internal command signal responsive to a second refresh signal; and

a refresh decoder operable to decode at least one internal command indicative of a refresh of the DRAM and causing the DRAM to be refreshed responsive thereto, the refresh decoder generating the first and second refresh signals during the refresh of the DRAM.

29. The dynamic random access memory of claim 28 wherein the first and second refresh signals comprise an auto-refresh signal.

30. The dynamic random access memory of claim 28 wherein the refresh decoder is further operable to removing the bias from the command signals and enabling the input buffers in the first set at the conclusion of the auto-refresh cycle.

31. The dynamic random access memory of claim 28, further comprising a clock input buffer through which an external clock signal may be applied to generate an internal clock signal, the clock input buffer being disabled by a third refresh signal, and wherein the refresh controller is operable to generate the third refresh signal during the refresh of the DRAM.

32. The dynamic random access memory of claim 28, further comprising a clock input buffer through which an external clock signal may be applied to generate an internal clock signal, and wherein the refresh controller is operable to terminate the first and second refresh signals responsive to a predetermined transition of the internal clock signal.

33. The dynamic random access memory of claim 32 wherein the refresh controller is operable to terminate the first and second refresh signals one-half the period of the clock signal after detecting the predetermined transition.

34. The dynamic random access memory of claim 32 wherein the refresh controller is operable to terminate the first and second refresh signals responsive to detecting a second transition of the clock signal having a polarity that is different from the polarity of the predetermined transition.

35. The dynamic random access memory of claim 28 wherein the bias circuit comprises a transistor coupled to an output terminal of an input buffer in the first set through which the at least one internal command signal is coupled.

36. The dynamic random access memory of claim 28 wherein the bias circuit is operable to bias a plurality of internal command signals to respective states that assert a no operation memory command.

37. The dynamic random access memory of claim 28 wherein the refresh decoder is further operable to detect the state of a predetermined command signal, and, in response to detecting a first state of the predetermined command signal, to continue biasing the command signal and disabling the input buffers in the first set at the conclusion of the auto-refresh cycle.

38. The dynamic random access memory of claim 37 wherein the refresh decoder is further operable to remove the bias from the command signal and enable the input

buffers in the first set responsive to detecting a transition of the predetermined command signal from the first state to a second state.

39. The dynamic random access memory of claim 37 wherein the refresh decoder is further operable to disable predetermined components of the dynamic random access memory at the conclusion of the auto-refresh cycle responsive to detecting a first state of the predetermined command signal.

40. The dynamic random access memory of claim 39 wherein the refresh decoder is further operable to enable the predetermined components of the dynamic random access memory in response to detecting a transition of the predetermined command signal from the first state to a second state.

42. The dynamic random access memory of claim 28 wherein the refresh decoder comprises:

a first decoder operable to decode the at least one internal command indicative of a refresh of the DRAM and to generate a predetermined refresh signal responsive thereto;

a timer coupled to the first decoder, the timer being triggered by the predetermined refresh signal and generating a refresh terminate signal a predetermined period after the predetermined refresh signal; and

a second decoder coupled to the first decoder and to the timer, the second decoder being operable to generate a refresh command and the first and second refresh signals responsive to the predetermined refresh signal, the second decoder further being operable to terminate the refresh command and the first and second refresh signals responsive to the refresh terminate signal.

43. The dynamic random access memory of claim 42 wherein the predetermined refresh signal comprises an auto-refresh signal and the refresh command comprises an auto-refresh command.

44. A dynamic random access memory ("DRAM"), comprising:

a row address circuit operable to receive and decode row address signals applied to an external terminal;

a column address circuit operable to receive and decode column address signals applied to an external terminal;

an array of dynamic random access memory cells operable to store data written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals;

a data path circuit operable to couple data signals corresponding to the data between the array and an external data terminal;

a clock input buffer through which an external clock signal is coupled to generate an internal clock signal;

a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to respective external terminals and coupled thorough a first set of input buffers to generate respective internal command signals, the input buffers in the first set being disabled by a first refresh signal, the command signal generator further including a bias circuit operable to bias at least one internal command signal responsive to a second refresh signal

a refresh decoder operable to decode at least an auto-refresh command and to initiate an auto-refresh cycle responsive thereto, the refresh decoder being further operable to detect the respective states of first and second predetermined command signals, the refresh decoder being operable to:

perform a self-refresh of the DRAM in response to decoding an auto-refresh command and detecting a first state of the first predetermined command signal and a first state of the second predetermined command signal;

perform an auto-refresh of the DRAM in response to decoding an auto-refresh command and a detecting second state of the first predetermined command signal and a first state of the second predetermined command signal;

perform an auto-refresh of the DRAM and generate the first and second refresh signals in response to decoding an auto-refresh command and detecting a first

state of the first predetermined command signal and a second state of the second predetermined command signal; and

perform an auto-refresh of the DRAM, generate the first and second refresh signals, and disable components of the DRAM other than the first set of input buffers at the conclusion of an auto-refresh cycle in response to decoding an auto-refresh command and detecting a second state of the first predetermined command signal and a second state of the second predetermined command signal.

45. The dynamic random access memory of claim 44 wherein the clock input buffer is disabled by a third refresh signal, and wherein the refresh decoder is further operable to generate the third refresh signal along with the first and second refresh signals.

46. The dynamic random access memory of claim 44 wherein the first predetermined signal comprises a clock enable signal.

47. The dynamic random access memory of claim 44 wherein the second predetermined signal comprises a data mask signal.

48. The dynamic random access memory of claim 44 wherein the refresh decoder is operable to terminate the first and second refresh signals at the conclusion of the auto-refresh if the first state of the first predetermined command signal and the second state of the second predetermined command signal were detected, the refresh decoder being further operable to continue generating the first and second refresh signals at the conclusion of the auto-refresh if the second state of the first predetermined command signal and the second state of the second predetermined command signal were detected.

49. The dynamic random access memory of claim 48 wherein the refresh decoder is operable to continue generating the first and second refresh signals at the conclusion of the auto-refresh as long as the second predetermined command signal is maintained in the second state.

50. The dynamic random access memory of claim 48 wherein the refresh decoder is operable to terminate the first and second refresh signals at the conclusion of the auto-refresh by detecting a predetermined transition of the internal clock signal, and to terminate the first and second refresh signals responsive to detecting the predetermined transition of the clock signal.

51. The dynamic random access memory of claim 44 wherein the bias circuit is operable to bias a plurality of internal command signals to generate a no operation memory command.

52. The dynamic random access memory of claim 44 wherein the refresh decoder comprises:

a first decoder operable to decode the at least one internal command indicative of a refresh of the DRAM and to generate a predetermined refresh signal responsive thereto;

a timer coupled to the first decoder, the timer being triggered by the predetermined refresh signal and generating a refresh terminate signal a predetermined period after the predetermined refresh signal; and

a second decoder coupled to the first decoder and to the timer, the second decoder being operable to generate a refresh command and the first and second refresh signals responsive to the predetermined refresh signal, the second decoder further being operable to terminate the refresh command and the first and second refresh signals responsive to the refresh terminate signal.

53. The dynamic random access memory of claim 44 wherein the bias circuit comprises a transistor coupled to an output terminal of an input buffer in the first set through which the at least one internal command signal is coupled

54. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system;

a memory controller generating a row address having a plurality of row address bits followed by a column address having a plurality of column address bits, the memory controller generating an array select signal prior to generating the plurality of column address bits, the array select signal corresponding to a column address bit and having either a first state or a second state; and

a memory device coupled to the memory controller, the memory device comprising:

a row address circuit operable to receive and decoder row address signals applied to an external terminal;

a column address circuit operable to receive and decoder column address signals applied to an external terminal;

an array of dynamic random access memory cells operable to store data written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals;

a data path circuit operable to couple data signals corresponding to the data between the array and an external data terminal;

a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to respective external terminals and coupled thorough a first set of input buffers to generate respective internal command signals, the input buffers in the first set being disabled by a first refresh signal, the command signal generator further including a bias circuit operable to bias at least one internal command signal responsive to a second refresh signal; and

a refresh decoder operable to decode at least one internal command indicative of a refresh of the DRAM and causing the DRAM to be refreshed responsive thereto, the refresh decoder generating the first and second refresh signals during the refresh of the DRAM.

55. The computer system of claim 54 wherein the first and second refresh signals comprise an auto-refresh signal.

56. The computer system of claim 54 wherein the refresh decoder is further operable to removing the bias from the command signals and enabling the input buffers in the first set at the conclusion of the auto-refresh cycle.

57. The computer system of claim 54, further comprising a clock input buffer through which an external clock signal may be applied to generate an internal clock signal, the clock input buffer being disabled by a third refresh signal, and wherein the refresh controller is operable to generate the third refresh signal during the refresh of the DRAM.

58. The computer system of claim 54, further comprising a clock input buffer through which an external clock signal may be applied to generate an internal clock signal, and wherein the refresh controller is operable to terminate the first and second refresh signals responsive to a predetermined transition of the internal clock signal.

59. The computer system of claim 54 wherein the bias circuit comprises a transistor coupled to an output terminal of an input buffer in the first set through which the at least one internal command signal is coupled.

60. The computer system of claim 54 wherein the refresh decoder is further operable to detect the state of a predetermined command signal, and, in response to detecting a first state of the predetermined command signal, to continue biasing the command signal and disabling the input buffers in the first set at the conclusion of the auto-refresh cycle.

61. The computer system of claim 54 wherein the refresh decoder comprises:

a first decoder operable to decode the at least one internal command indicative of a refresh of the DRAM and to generate a predetermined refresh signal responsive thereto;

a timer coupled to the first decoder, the timer being triggered by the predetermined refresh signal and generating a refresh terminate signal a predetermined period after the predetermined refresh signal; and

a second decoder coupled to the first decoder and to the timer, the second decoder being operable to generate a refresh command and the first and second refresh signals responsive to the predetermined refresh signal, the second decoder further being operable to terminate the refresh command and the first and second refresh signals responsive to the refresh terminate signal.

62. The computer system of claim 61 wherein the predetermined refresh signal comprises an auto-refresh signal and the refresh command comprises an auto-refresh command.

63. A computer system, comprising:

a processor having a processor bus;

an input device coupled to the processor through the processor bus adapted to allow data to be entered into the computer system;

an output device coupled to the processor through the processor bus adapted to allow data to be output from the computer system;

a memory controller generating a row address having a plurality of row address bits followed by a column address having a plurality of column address bits, the memory controller generating an array select signal prior to generating the plurality of column address bits, the array select signal corresponding to a column address bit and having either a first state or a second state; and

a memory device coupled to the memory controller, the memory device comprising:

a row address circuit operable to receive and decoder row address signals applied to an external terminal;

a column address circuit operable to receive and decoder column address signals applied to an external terminal;

an array of dynamic random access memory cells operable to store data written to or read from the array at a location determined by the decoded row address signals and the decoded column address signals;

a data path circuit operable to couple data signals corresponding to the data between the array and an external data terminal;

a clock input buffer through which an external clock signal is coupled to generate an internal clock signal;

a command signal generator operable to generate a sequence of control signals corresponding to command signals applied to respective external terminals and coupled thorough a first set of input buffers to generate respective internal command signals, the input buffers in the first set being disabled by a first refresh signal, the command signal generator further including a bias circuit operable to bias at least one internal command signal responsive to a second refresh signal; and

a refresh decoder operable to decode at least an auto-refresh command and to initiate an auto-refresh cycle responsive thereto, the refresh decoder being further operable to detect the respective states of first and second predetermined command signals, the refresh decoder being operable to:

perform a self-refresh of the DRAM in response to decoding an auto-refresh command and detecting a first state of the first predetermined command signal and a first state of the second predetermined command signal;

perform an auto-refresh of the DRAM in response to decoding an auto-refresh command and a detecting second state of the first predetermined command signal and a first state of the second predetermined command signal;

perform an auto-refresh of the DRAM and generate the first and second refresh signals in response to decoding an auto-refresh command and detecting a first state of the first predetermined command signal and a second state of the second predetermined command signal; and

perform an auto-refresh of the DRAM, generate the first and second refresh signals, and disable components of the DRAM other than the

first set of input buffers at the conclusion of an auto-refresh cycle in response to decoding an auto-refresh command and detecting a second state of the first predetermined command signal and a second state of the second predetermined command signal.

64. The computer system of claim 63 wherein the clock input buffer is disabled by a third refresh signal, and wherein the refresh decoder is further operable to generate the third refresh signal along with the first and second refresh signals.

65. The computer system of claim 63 wherein the first predetermined signal comprises a clock enable signal.

66. The computer system of claim 63 wherein the second predetermined signal comprises a data mask signal.

67. The computer system of claim 63 wherein the refresh decoder is operable to terminate the first and second refresh signals at the conclusion of the auto-refresh if the first state of the first predetermined command signal and the second state of the second predetermined command signal were detected, the refresh decoder being further operable to continue generating the first and second refresh signals at the conclusion of the auto-refresh if the second state of the first predetermined command signal and the second state of the second predetermined command signal were detected.

68. The computer system of claim 63 wherein the refresh decoder is operable to continue generating the first and second refresh signals at the conclusion of the auto-refresh as long as the second predetermined command signal is maintained in the second state.

69. The computer system of claim 67 wherein the refresh decoder is operable to terminate the first and second refresh signals at the conclusion of the auto-refresh

by detecting a predetermined transition of the internal clock signal, and to terminate the first and second refresh signals responsive to detecting the predetermined transition of the clock signal.

70. The computer system of claim 63 wherein the bias circuit is operable to bias a plurality of internal command signals to generate a no operation memory command.

71. The computer system of claim 63 wherein the refresh decoder comprises:

a first decoder operable to decode the at least one internal command indicative of a refresh of the DRAM and to generate a predetermined refresh signal responsive thereto;

a timer coupled to the first decoder, the timer being triggered by the predetermined refresh signal and generating a refresh terminate signal a predetermined period after the predetermined refresh signal; and

a second decoder coupled to the first decoder and to the timer, the second decoder being operable to generate a refresh command and the first and second refresh signals responsive to the predetermined refresh signal, the second decoder further being operable to terminate the refresh command and the first and second refresh signals responsive to the refresh terminate signal.

72. The computer system of claim 63 wherein the bias circuit comprises a transistor coupled to an output terminal of an input buffer in the first set through which the at least one internal command signal is coupled

73. A method of performing an auto-refresh of a dynamic random access memory having a first set of input buffers through which command signals are coupled, the method comprising:

disabling the input buffers in the first set during the performance of the auto-refresh cycle;

biasing a plurality of command signals to assert a predetermined memory command during the auto-refresh cycle;

at the conclusion of the auto-refresh cycle, removing the bias from the command signals and enabling the input buffers in the first set.

74. The method of claim 73 wherein the dynamic random access memory comprises a synchronous dynamic random access memory that operates in synchronism with a clock signal applied to the dynamic random access memory through a clock input buffer.

75. The method of claim 74, further comprising disabling the clock input buffer during at least a portion of the auto-refresh cycle and re-enabling the clock input buffer at the conclusion of the auto-refresh cycle.

76. The method of claim 75 wherein the act of removing the bias of the command signals and enabling the input buffers in the first set comprises:

examining the clock signal coupled through the clock input buffer;

detecting a predetermined transition of the clock signal; and

removing the bias from the command signals and enabling the input buffers in the first set responsive to detecting a predetermined transition of the clock signal.

77. The method of claim 76 wherein the act of removing the bias from the command signals and enabling the input buffers in the first set responsive to detecting a predetermined transition of the clock signal further comprises waiting a predetermined duration after detecting the predetermined transition to remove the bias from the command signals and enable the input buffers in the first set.

78. The method of claim 77 wherein the act of waiting a predetermined duration after detecting the predetermined transition comprises waiting for one-half the period of the clock signal after detecting the predetermined transition.

79. The method of claim 77 wherein the act of waiting a predetermined duration after detecting the predetermined transition comprises waiting for a second transition of the clock signal having a polarity that is different from the polarity of the predetermined transition.

80. The method of claim 79 wherein the predetermined transition comprises a rising edge of the clock signal applied to the clock input buffer, and the second transition comprises a falling edge of the clock signal applied to the clock input buffer.

81. The method of claim 73 wherein the act of biasing a plurality of command signals to assert a predetermined memory command during the auto-refresh cycle comprises biasing a plurality of command signals to assert a no operation memory command during the auto-refresh cycle.

82. The method of claim 73, further comprising:

detecting the state of a command signal;

in response to detecting a first state of the command signal, continuing to bias the command signals and disable the input buffers in the first set at the conclusion of the auto-refresh cycle; and

in response to detecting a transition of the command signal from the first state to a second state, removing the bias from the command signals and enabling the input buffers in the first set.

83. The method of claim 82, further comprising:

in response to detecting a first state of the command signal, disabling predetermined components of the dynamic random access memory at the conclusion of the auto-refresh cycle; and

in response to detecting a transition of the command signal from the first state to a second state, enabling the predetermined components of the dynamic random access memory.

84. The method of claim 73 wherein the dynamic random access memory further includes a second set of input buffers through which address signals are coupled, and wherein the method further comprises:

disabling the input buffers in the second set during the performance of the auto-refresh cycle; and

at the conclusion of the auto-refresh cycle, enabling the input buffers in the second set.

85. A method of reducing power consumption in a dynamic random access memory ("DRAM") having a first set of input buffers through which command signals are coupled, the method comprising:

detecting each of a plurality of memory commands, including an auto-refresh command;

detecting the state of a first predetermined command signal;

in response to detecting an auto-refresh command and a first state of the first predetermined command signal, performing an auto-refresh of the DRAM and, at the conclusion of the auto-refresh, automatically transitioning the DRAM to an active mode; and

in response to detecting an auto-refresh command and a second state of the first predetermined command signal, performing an auto-refresh of the DRAM and, at the conclusion of the auto-refresh, automatically transitioning the DRAM to a low power precharge mode.

86. The method of claim 85 wherein the first predetermined signal comprises a clock enable signal.

87. The method of claim 85 wherein the DRAM comprises a synchronous dynamic random access memory that operates in synchronism with a clock signal applied to the DRAM through a clock input buffer.

88. The method of claim 87, further comprising disabling the clock input buffer during at least a portion of the auto-refresh and re-enabling the clock input buffer at the conclusion of the auto-refresh in the event the first state of the first predetermined command signal is detected.

89. The method of claim 85 wherein the act of performing an auto-refresh of the DRAM comprises disabling the input buffers in the first set during the performance of the auto-refresh.

90. The method of claim 89, wherein the act of performing an auto-refresh of the DRAM further comprises biasing a plurality of command signals to assert a predetermined memory command during the auto-refresh.

91. The method of claim 90, wherein the act of performing an auto-refresh of the DRAM further comprises removing the bias from the command signals and enabling the input buffers in the first set at the conclusion of the auto-refresh cycle.

92. The method of claim 91, wherein the DRAM further includes a clock input buffer that receives an external clock signal to generate an internal clock signal, and wherein the act of removing the bias from the command signals and enabling the input buffers in the first set comprises:

examining the internal clock signal;

detecting a predetermined transition of the internal clock signal; and

removing the bias from the command signals and enabling the input buffers in the first set responsive to detecting a predetermined transition of the internal clock signal.

93. The method of claim 92 wherein the act of removing the bias from the command signals and enabling the input buffers in the first set responsive to detecting a predetermined transition of the internal clock signal further comprises waiting a

predetermined duration after detecting the predetermined transition to remove the bias from the command signals and enable the input buffers in the first set.

94. The method of claim 93 wherein the act of waiting a predetermined duration after detecting the predetermined transition comprises waiting for one-half the period of the clock signal after detecting the predetermined transition.

95. The method of claim 93 wherein the act of waiting a predetermined duration after detecting the predetermined transition comprises waiting for a second transition of the clock signal having a polarity that is different from the polarity of the predetermined transition.

96. The method of claim 90 wherein the act of biasing a plurality of command signals to assert a predetermined memory command during the auto-refresh comprises biasing a plurality of command signals to assert a no operation memory command during the auto-refresh.

97. The method of claim 89 wherein the DRAM further includes a second set of input buffers through which address signals are coupled, and wherein the method further comprises:

disabling the input buffers in the second set during the performance of the auto-refresh; and

at the conclusion of the auto-refresh, enabling the input buffers in the second set.

98. The method of claim 85 wherein the act of automatically transitioning the DRAM to a low power precharge mode comprises disabling predetermined components of the dynamic random access memory at the conclusion of the auto-refresh.

99. The method of claim 98, further comprising enabling the predetermined components of the dynamic random access memory in response to detecting a transition of the command signal from the second state to the first state.

100. A method of reducing power consumption in a synchronous dynamic random access memory ("SDRAM") having a first set of input buffers through which command signals are coupled and a clock input buffer through which a clock signal is coupled, the method comprising:

detecting each of a plurality of memory commands, including an auto-refresh command;

detecting the state of a first predetermined command signal;

detecting the state of a second predetermined command signal;

in response to detecting an auto-refresh command and a first state of the first predetermined command signal and a first state of the second predetermined command signal, performing a self-refresh of the SDRAM;

in response to detecting an auto-refresh command and a second state of the first predetermined command signal and a first state of the second predetermined command signal, performing an auto-refresh of the SDRAM;

in response to detecting an auto-refresh command and a first state of the first predetermined command signal and a second state of the second predetermined command signal, performing a low power auto-refresh of the SDRAM, the low power auto-refresh comprising disabling the input buffers in the first set and biasing a plurality of command signals to assert a predetermined memory command during the auto-refresh cycle; and

in response to detecting an auto-refresh command and a second state of the first predetermined command signal and a second state of the second predetermined command signal, performing a low power auto-refresh of the SDRAM and, at the conclusion of the auto-refresh, performing a low power precharge of the SDRAM, the low power precharge comprising disabling components of the SDRAM other than the first set of input buffers.

101. The method of claim 100 wherein the act of performing a low power auto-refresh of the SDRAM further comprises disabling the clock input buffer during at least a portion of the low power auto-refresh

102. The method of claim 101, further comprising re-enabling the clock input buffer at the conclusion of the auto-refresh in the event the first state of the first predetermined command signal is detected.

103. The method of claim 100, further comprising:

removing the bias from the command signals and enabling the input buffers in the first set at the conclusion of the low power auto-refresh if the first state of the first predetermined command signal and the second state of the second predetermined command signal were detected; and

maintaining the bias to the command signals and continuing to disable the input buffers in the first set at the conclusion of the low power auto-refresh if the second state of the first predetermined command signal and the second state of the second predetermined command signal were detected.

104. The method of claim 103 wherein the act of maintaining the bias of the command signals and continuing to disable the input buffers in the first set at the conclusion of the low power auto-refresh comprises maintaining the bias of the command signals and continuing to disable the input buffers in the first set as long as the second predetermined command signal is maintained in the second state.

105. The method of claim 103 wherein the act of removing the bias from the command signals and enabling the input buffers in the first set at the conclusion of the low power auto-refresh comprises:

examining the clock signal coupled through the clock input buffer;

detecting a predetermined transition of the clock signal; and

removing the bias from the command signals and enabling the input buffers in the first set responsive to detecting a predetermined transition of the clock signal.

106. The method of claim 105 wherein the act of removing the bias from the command signals and enabling the input buffers in the first set responsive to detecting a predetermined transition of the clock signal further comprises waiting a predetermined duration after detecting the predetermined transition to remove the bias from the command signals and enable the input buffers in the first set.

107. The method of claim 106 wherein the act of waiting a predetermined duration after detecting the predetermined transition comprises waiting for one-half the period of the clock signal after detecting the predetermined transition.

108. The method of claim 106 wherein the act of waiting a predetermined duration after detecting the predetermined transition comprises waiting for a second transition of the clock signal having a polarity that is different from the polarity of the predetermined transition.

109. The method of claim 100 wherein the act of biasing a plurality of command signals to assert a predetermined memory command during the auto-refresh cycle comprises biasing a plurality of command signals to assert a no operation memory command during the auto-refresh cycle.

110. The method of claim 100 wherein the first predetermined signal comprises a clock enable signal.

111. The method of claim 100 wherein the second predetermined signal comprises a data mask signal.